Transistor for active matrix display and a method for producing said transistor

The invention relates to a transistor for active matrix display, a display unit comprising the said transistor and a method for producing the said transistor.

Since the advent of the portables and the need for flat display panels, electronic displays implementing thin-film transistor technology and liquid crystals have experienced a phenomenal growth, to the point where full-colour displays have been realised that can compete with cathode ray tube displays. Amorphous silicon thin-film transistors are extensively used as pixel charging devices in active matrix liquid crystal displays, principally because of its application to large glass substrates, low cost and remarkable matching with the requirements of liquid crystal driving. Over the last decade, a rapidly growing demand for high information content displays offering high performances (excellent contrast, homogeneity of colours, high luminance, large viewing angles...) and having sizes down to "micro-panel", for mobile phones for example, has nonetheless raised a huge interest for new technologies like organic light emissive diodes (OLED), polymer material based light emissive diodes (PLED), ... The response time of OLED devices makes them perfectly suitable for video rate.

This demand adds constraints on the active material used in thin film transistors for active matrix displays, namely a higher stability and a more rapid charging than amorphous silicon (a-Si:H) thin films can provide. It is also necessary for a higher integration and to further reduce the cost of the display to process the driving circuits directly on the glass panel instead of connecting external circuits.

It is known that microcrystalline silicon (μc-Si:H) is compatible with amorphous silicon technology and can be directly deposited using plasma deposition technology at low temperatures without further thermal or laser treatment.

However, up to date studies of μc-Si:H thin films {ROCA I CABARROCAS, P et al.; J. Appl. Phys. **86** (1999) 7079 and references cited therein} have only reported linear mobilities similar to those of a-

Si:H thin film transistors. Therefore, no improvement would be expected from these studies on the charging time of pixels using said μc-Si:H thin film transistors and on the driving circuit integration.

The purpose of the invention is hence to remedy the shortcomings mentioned above and to propose a transistor for active matrix display having one or more of the following features and advantages: namely, a high field effect mobility, an excellent threshold voltage stability, a high level of drive circuit integration and a high duty ratio, offering a low cost transistor for pixel-charging devices used in active matrix displays.

In addition, the invention has as an objective a method for producing a transistor for active matrix display, this method being at once rapid and easy to implement, in particular, in industrial transistor manufacturing devices.

To this end, the invention concerns a transistor for active matrix display comprising a microcrystalline silicon film and an insulator, the crystalline fraction being above 80%.

According to the invention, said transistor comprises a plasma treated interface located between the insulator and the microcrystalline silicon film so that the said transistor has a linear mobility equal or superior to 1.5 $cm^2V^{-1}s^{-1}$ and shows threshold voltage stability.

The microcrystalline silicon film is composed of a mixture of amorphous tissue and crystallites that are crystallised grains. We shall call hereinafter "Crystalline fraction", the ratio by volume of the said grains. At a crystalline fraction of 100%, microcrystalline silicon films without any amorphous phase are achieved. In other words, the thin film is fully crystallised.

We shall call hereinafter "Threshold voltage stability", a threshold voltage shift equal or inferior to 0.5 V with time when the thin film transistor is submitted to a bias stress. Typical stress tests are performed for example under a gate voltage of 30 V and at a substrate temperature of 60°C.

According to various embodiments, the present invention also concerns the characteristics below, considered individually or in all their technical possible combinations.

- the microcrystalline silicon film comprises grains whose size ranges between 10 nm and 400 nm,
- said grain size ranges between 100 nm and 200 nm,
- the microcrystalline silicon film thickness is comprised between 100 nm and 450 nm,
- said transistor has a top-gate electrode,
- said transistor has a bottom-gate electrode,
- the microcrystalline silicon film is produced by hot wire technique,
- the microcrystalline silicon film is produced by radiofrequency glow discharge technique.

The invention concerns as well a display unit having a line-column matrix of pixels that are actively addressed. According to the invention, each pixel comprises at least a transistor as previously described.

According to various embodiments, the present invention also concerns the characteristics below, considered individually or in all their technical possible combinations.

- said pixels comprise light emissive organic materials,
- said pixels comprise liquid crystals,
- said pixels comprise light emissive polymer materials,
- electronic control means to drive each pixel are at least partially integrated on the corresponding microcrystalline silicon film.

The display unit described above can be advantageously applied with a device selected from the group comprising a computer, a video camera, a digital camera, a portable terminal, a player for recorder media, an electronic game equipment and a projector.

The invention concerns as well a method for producing a transistor for active matrix display comprising the steps of forming an active material and electrodes, said active material being formed using vapor deposition methods and said transistor comprising an insulator.

According to the invention,

- one forms a plasma treated interface on top of said insulator,

and

- one forms a microcrystalline film on top of said treated interface at a temperature comprised between 100 and 400°C using at least a deposition chemical element and a crystallisation chemical element.

According to various embodiments, the present invention also concerns the characteristics below, considered individually or in all their technical possible combinations.

- said plasma treated interface is selected from the group consisting of a SiN_x layer, a SiN_xO_y layer, a SiO_2 layer and glass,
- one forms the plasma treated interface using a gas selected from the group consisting of N_2, O_2, N_2O and NH_3,

The insulator is treated by plasma deposition to form a plasma treated interface so as to reduce the density of nucleation sites.

- the microcrystalline silicon film is formed using a buffer gas selected from the group consisting of Ar, Xe, Kr and He,
- said crystallisation chemical elements is H_2,
- said deposition chemical elements are selected among the group comprising SiH_4, SiF_4,
- said deposition chemical elements flux and said crystallisation chemical elements flux are at equilibrium during the growth of the microcrystalline silicon film,
- one forms a top gate transistor,
- one patterns a substrate comprising a metallic layer to form source and drain electrodes,
- one forms a bottom gate transistor,
- a substrate comprises a gate electrode,
- the microcrystalline silicon film comprises grains whose size ranges between 10 nm and 400 nm,
- the microcrystalline silicon film thickness is comprised between 100 nm and 450 nm,
- the vapor deposition methods use radiofrequency glow discharge technique,
- one uses a 13.56 MHz PECVD reactor.

A "13.56 MHz PECVD reactor" means here a reactor powered by radiofrequency energy at a frequency of 13.56 MHz used with a plasma enhanced chemical vapour deposition method.

To facilitate further description of the invention, the following drawings are provided in which:

Figure 1 is a schematic view of a thin film transistor structure for a bottom gate transistor according to the invention.

Figure 2 shows the experimental values obtained as a function of the percolation thickness (nm) for the linear mobility of a µc-Si:H thin film produced from SiF_4-Ar-H_2 mixtures.

Figure 3 shows an atomic force microscopy relief of a µc-Si:H thin film produced from SiF_4-Ar-H_2 mixtures. The µc-Si:H thin film was formed on a SiN_x thin film treated with an Ar plasma. The image extends laterally over an area of 2 x 2 μm^2.

Figure 4 shows an atomic force microscopy relief of a µc-Si:H thin film produced from SiF_4-Ar-H_2 mixtures. The µc-Si:H thin film was formed on a SiN_x thin film treated with an N_2 plasma. The image extends laterally over an area of 5 x 5 μm^2.

These drawings are provided for illustrative purposes only and should not be used to unduly limit the scope of the invention.

The invention concerns a method for producing a transistor 1 for active matrix display comprising the steps of forming an active material and electrodes 2, said active material being formed using vapor deposition methods and said transistor 1 comprising an insulator 3. The vapor deposition methods use, for example, radiofrequency glow discharge technique. In a particular embodiment, one uses a 13.56 MHz PECVD reactor. However, said reactor can be powered by radiofrequency energy at another frequency. The vapor deposition methods can implement also a microwave ECR (electron cyclotron resonance) technique.

According to the invention, one forms a plasma treated interface 4 on top of said insulator 3. In a preferred embodiment, said treated interface 4 is selected from the group consisting of a SiN_x layer, a SiN_xO_y layer, a SiO_2 layer and glass. The plasma treated interface 4 can be formed using a gas selected from the group consisting of N_2, O_2, N_2O and NH_3.

One then forms on top of said treated interface 4, a microcrystalline film 5 at a temperature comprised between 100 and 400°C using at least a deposition chemical element and a crystallisation chemical element. Said crystallisation chemical element is said to

promote the crystallisation of the μc-Si:H thin film 5 and is, for example, H_2. The crystallisation chemical element and the deposition element can be deposited together or alternately with time. The deposition chemical elements are selected among the group comprising SiH_4, SiF_4. A buffer gas can be added to optimise the plasma conditions, said gas being chosen from the group consisting of Ar, Xe, Kr and He.

In a particular implementation, hydrogen is used through plasma deposition as a crystallisation element for the formation of μc-Si:H films. The hydrogen plasma exposure of a-Si:H films formed from pure silane crystallises said a-Si:H films through its surface and subsurface reactions. The method then consists in repeating many times the deposition of a-Si:H during a time τ_1 followed by its exposure to a hydrogen plasma during a time τ_2. The μc-Si:H thin film is said to be formed by plasma deposition from a SiH_4, H_2 mixture. In a preferred embodiment, the deposition chemical elements flux and the crystallisation chemical elements flux are at equilibrium during the growth of the microcrystalline silicon film 5.

The microcrystalline silicon film 5 has a thickness which is comprised between 100 nm and 450 nm and comprises grains 6 whose size ranges between 10 nm and 400 nm.

For the preparation of either bottom gate or top gate transistors, the microcrystalline silicon film 5 is grown on an insulator 3. High mobility microcrystalline silicon 5 is obtained when the insultor 3 is treated so that the density of nucleation sites is reduced. This treatment can be achieved either for bottom gate or for top gate transistors.

In a first embodiment, a top gate transistor is formed, one patterns a substrate comprising a metallic or a TCO (transparent conductive oxyde) layer to form source and drain electrodes 2.

In a second embodiment, one forms a bottom gate transistor and the substrate comprises a gate electrode 2.

The invention also concerns a transistor 1 for active matrix display. Figure 1 shows the said transistor 1 according to a particular embodiment of the invention. It comprises a microcrystalline silicon film 5 and an insulator 3, the crystalline fraction being above 80%. The transistor 1 for active matrix display also comprises a plasma treated

interface 4 located between the insulator 3 and the microcrystalline silicon film 5 so that the said transistor 1 has a linear mobility equal or superior to 1.5 $cm^2V^{-1}s^{-1}$ and shows threshold voltage stability. Preferentially the crystalline fraction is higher than 85% since an excellent voltage stability is then achieved (the shift is less than 0.15 V).

According to the current understanding of said transistor 1 structure, the formation of a plasma treated interface 4 reduces the density of nucleation sites, thus allowing the lateral growth of crystallites 6. Said growth leads to the formation of large grains 6 resulting in a measured higher mobility.

Said microcrystalline silicon film 5 can be produced by hot wire technique or by radiofrequency glow discharge technique.

The microcrystalline silicon film 5 contains crystallites 6 that are crystallised grains 6 having a size ranging between 10 nm and 400 nm. Advantageously, the grain size ranges between 100 nm and 200 nm.

In an embodiment, the microcrystalline silicon film 5 thickness is comprised between 100 nm and 450 nm, and preferentially is comprised between 100 nm and 150 nm to have a low OFF current. A low off current, besides a high linear mobility and stability, is required for an industrial application since it determines the image quality in the electro-optic transducer (liquid crystal display, organic electroluminescent display, ...).

Figure 1 shows a thin film transistor 1 for active matrix display having a bottom-gate electrode, but the transistor 1 can also be realised with a top-gate electrode.

The invention further concerns a display unit having a line-column matrix of pixels comprising at least a transistor 1 as previously described. Said pixels are actively addressed which means that the matrix-type display is scanned line by line over the frame time and a current is supplied to said pixels during the whole frame time. This addressing method makes it perfectly suitable to pixels comprising light emissive organic or polymer materials. It can be advantageously used for pixels comprising liquid crystals. In a preferred embodiment, electronic control means to drive each pixel are at least partially integrated on the

corresponding display panel. Hence, the number of external driving circuits is reduced.

The transistor for active matrix display and the method for producing the said transistor according to the invention have been the object of various implementations whose following examples demonstrate the quality of the results obtained.

EXAMPLE 1

The method for producing a transistor 1 according to the invention has been first implemented to study a bottom gate thin film transistor produced from SiF_4-Ar-H_2 mixtures. Figure 2 shows the experimental (circles, respectively inverted triangles) values obtained as a function of the "percolation thickness" (nm) 7 for the linear mobility ($cm^2V^{-1}s^{-1}$) 8 of said µc-Si:H thin film transistor. The "percolation thickness" is a parameter which is defined as the thickness at which the crystalline fraction in the film reaches 100%. The dashed line 9 (respectively solid line 10) is only shown to provide a guide line to the eye.

The circle values 11 were obtained for a µc-Si:H thin film formed by plasma deposition on a SiN_x substrate under a total pressure of 1 Torr of SiF_4-Ar-H_2 mixtures and an RF power of 240 mW/cm^2 for 35 minutes. The inverted triangle values 12 were obtained for a µc-Si:H thin film formed by plasma deposition at a RF power of 280 mW/cm^2. The pressure of said mixture was 1.5 Torr. The square value 13 was obtained for a µc-Si:H thin film formed by submitting a SiNx substrate to a SiF_4-Ar-H_2 mixture plasma treatment under a total pressure of 1 Torr and an RF power of 280 mW/cm^2 for 60 minutes. All these depositions were performed at a temperature of 200°C.

From these experimental values, there is a clear tendency for both series of samples to an increase of the mobility with the increase of the percolation thickness. Hence, despite of having a slow crystallisation velocity, films that end up being fully crystallised have the highest mobilities. Thin film transistors having a mobility of 3 $cm^2/V.s.$ are reported.

EXAMPLE 2

Figure 3 shows an atomic force microscopy (AFM) relief of a µc-Si:H thin film 5. The µc-Si:H thin film 5 was formed by submitting a SiN_x thin film 3 to an Ar plasma and then to a SiF_4-Ar-H_2 mixture plasma treatment. The image extends laterally over an area of 5 x 5 μm^2. Measurements of the thin film transistor realised with said µc-Si:H thin film show values for the linear mobility of the order of 0.02 $cm^2/V.s$. This AFM image clearly shows small crystallites 6 having a mean size less than 80 nm.

Figure 4 shows an atomic force microscopy relief of a µc-Si:H thin film produced from a SiF_4-Ar-H_2 mixture. The µc-Si:H thin film was formed on a SiN_x thin film submitted to a N_2 treatment. The image extends laterally over an area of 2 x 2 μm^2. Measurements of the thin film transistor realised with said µc-Si:H thin film show values for the linear mobility of the order of 3 $cm^2/V.s$. This AFM image clearly shows small crystallites having a mean size of the order of 400 nm.

The formation of a plasma treated SiN_x interface 4 on top of the SiN_x layer 3 before the µc-Si:H thin film 5 deposition clearly promotes the deposition of large grain 6 materials at low temperatures. The linear mobility of the film obtained is then shown to be superior to 2 $cm^2/V.s$.

CLAIMS

1. A transistor for active matrix display comprising a microcrystalline silicon film (5) and an insulator (3), the crystalline fraction being above 80%,

wherein it comprises a plasma treated interface (4) located between the insulator (3) and the microcrystalline silicon film (5) so that the said transistor (1) has a linear mobility equal or superior to 1.5 $cm^2V^{-1}s^{-1}$, shows threshold voltage stability and wherein the microcrystalline silicon film (5) comprises grains (6) whose size ranges between 10 nm and 400 nm.

2. A transistor for active matrix display according to claim 1, wherein said grain size ranges between 100 nm and 200 nm.

3. A transistor for active matrix display according to claim 1 or 2, wherein the microcrystalline silicon film (5) thickness is comprised between 100 nm and 450 nm.

4. A transistor for active matrix display according to any one of claims 1 to 3, wherein said transistor (1) has a top-gate electrode.

5. A transistor for active matrix display according to any one of claims 1 to 3 wherein said transistor (1) has a bottom-gate electrode.

6. A display unit having a line-column matrix of pixels that are actively addressed, wherein each pixel comprises at least a transistor (1) according to any one of claims 1 to 5.

7. A display unit according to claim 6, wherein said pixels comprise light emissive organic materials.

8. A display unit according to claim 6, wherein said pixels comprise liquid crystals.

9. A display unit according to claim 6, wherein said pixels comprise light emissive polymer materials.

10. A display unit according to any one of claims 6 to 9, wherein electronic control means to drive each pixel are at least partially integrated on the corresponding microcrystalline silicon film.

11. A method for producing a transistor for active matrix display comprising the steps of forming an active material and electrodes (2), said active material being formed using vapor deposition methods and said transistor (1) comprising an insulator (3),

wherein,

- forming a plasma treated interface (4) on top of said insulator (3), and

- forming a microcrystalline film (5) on top of said treated interface (4) at a temperature comprised between 100 and 400°C using at least a deposition chemical element and a crystallisation chemical element wherein the said crystalline fraction being above 80% and said microcrystalline silicon film (5) comprises grains (6) where size ranges between 10 nm and 400 nm.

12. A method for producing a transistor according to claim 11, wherein said plasma treated interface (4) is selected from the group consisting of a SiN_x layer, a SiN_xO_y layer, a SiO_2 layer and glass.

13. A method for producing a transistor according to claim 12, wherein one forms the plasma treated interface (4) using a gas selected from the group consisting of N_2, O_2, N_2O and NH_3.

14. A method for producing a transistor according to one of claims 11 to 13, wherein the microcrystalline silicon film (5) is formed using a buffer gas selected from the group consisting of Ar, Xe, Kr and He.

15. A method for producing a transistor according to any of the claims 11 to 14, wherein said crystallisation chemical elements is H_2.

16. A method for producing a transistor according to one of claims 11 to 15, wherein said deposition chemical elements are selected among the group comprising SiH_4, SiF_4.

17. A method for producing a transistor according to one of claims 11 to 16, wherein said deposition chemical elements flux and said crystallisation chemical elements flux are at equilibrium during the growth of the microcrystalline silicon film.

18. A method for producing a transistor according to any one of claims 11 to 17, wherein one forms a top gate transistor.

19. A method for producing a transistor according to claim 18, wherein one patterns the substrate comprising a metallic layer to form source and drain electrodes.

20. A method for producing a transistor according to any one of claims 11 to 17, wherein one forms a bottom gate transistor.

21. A method for producing a transistor according to claim 20, wherein the substrate comprises a gate electrode.

22. A method for producing a transistor according to any one of claims 11 to 21, wherein the microcrystalline silicon film (5) comprises grains (6) whose size ranges between 10 nm and 400 nm.

23. A method for producing a transistor according to any one of claims 11 to 22, wherein the microcrystalline silicon film (5) thickness is comprised between 100 nm and 450 nm.

24. A method for producing a transistor according to any one of claims 11 to 23, wherein the microcrystalline silicon film (5) is produced by hot wire technique.

25. A method for producing a transistor according to any one of claims 11 to 24, wherein the microscrystalline silicon film (5) is produced by radiofrequency glow discharge technique.

26. A method for producing a transistor according to any one of claims 11 to 25, wherein the vapor deposition methods use radiofrequency glow discharge technique.

27. A method for producing a transistor according to claim 26, wherein one uses a 13.56 MHz PECVD reactor.

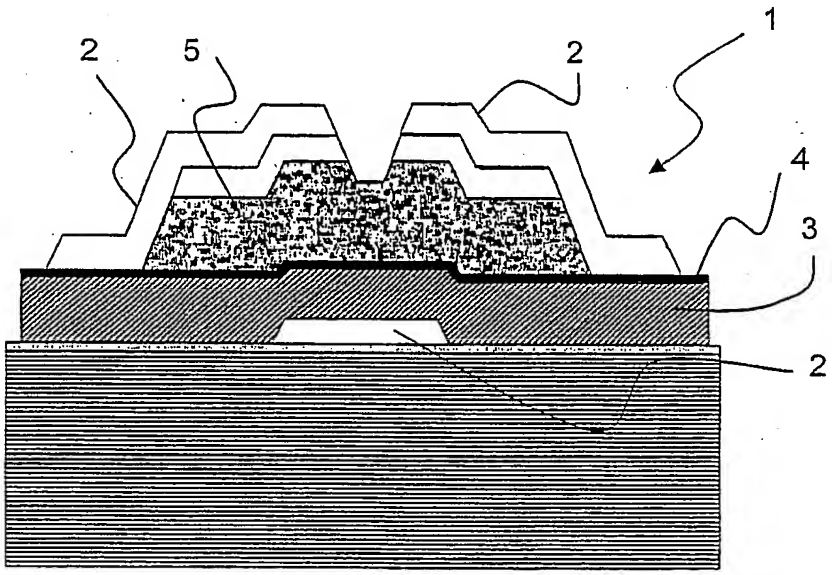
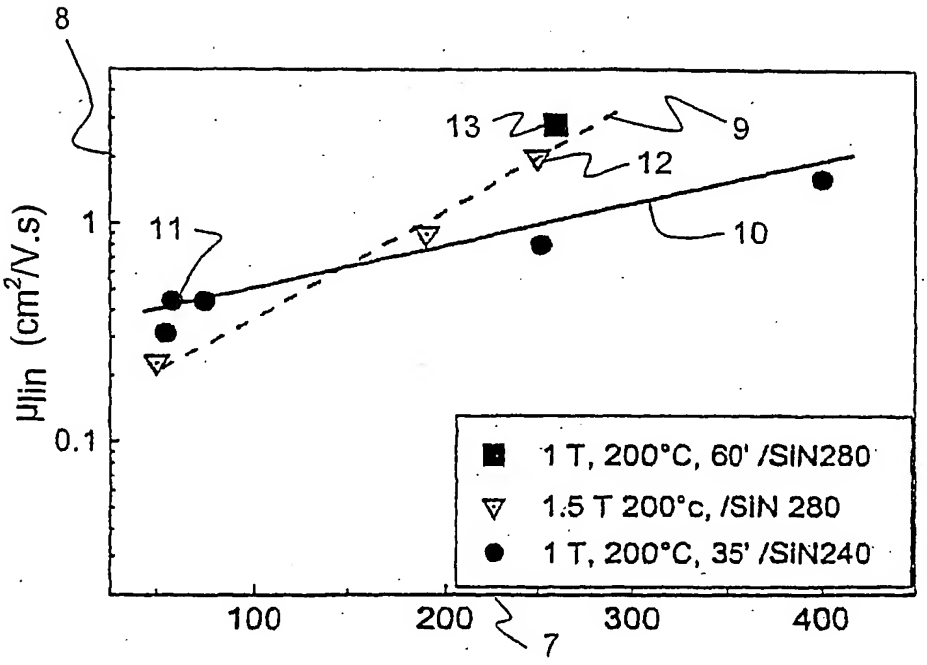


FIGURE 1


8
13
9
12
11
10
1
0.1
μlin (cm²/V.s)
100
200
300
400
7
1 T, 200°C, 60' /SiN280
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1 T, 200°C, 35' /SiN240

FIGURE 2

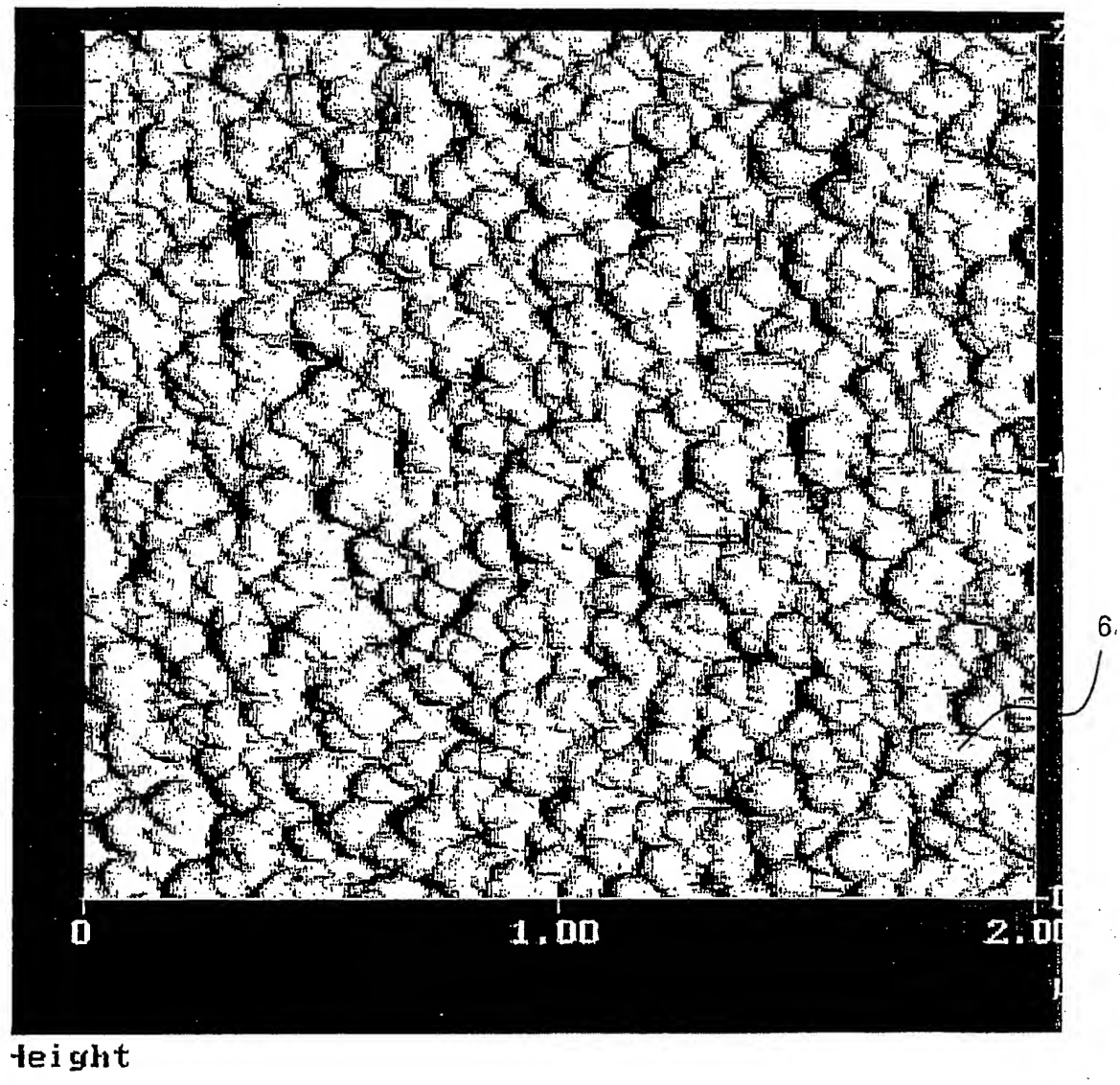

FIGURE 3

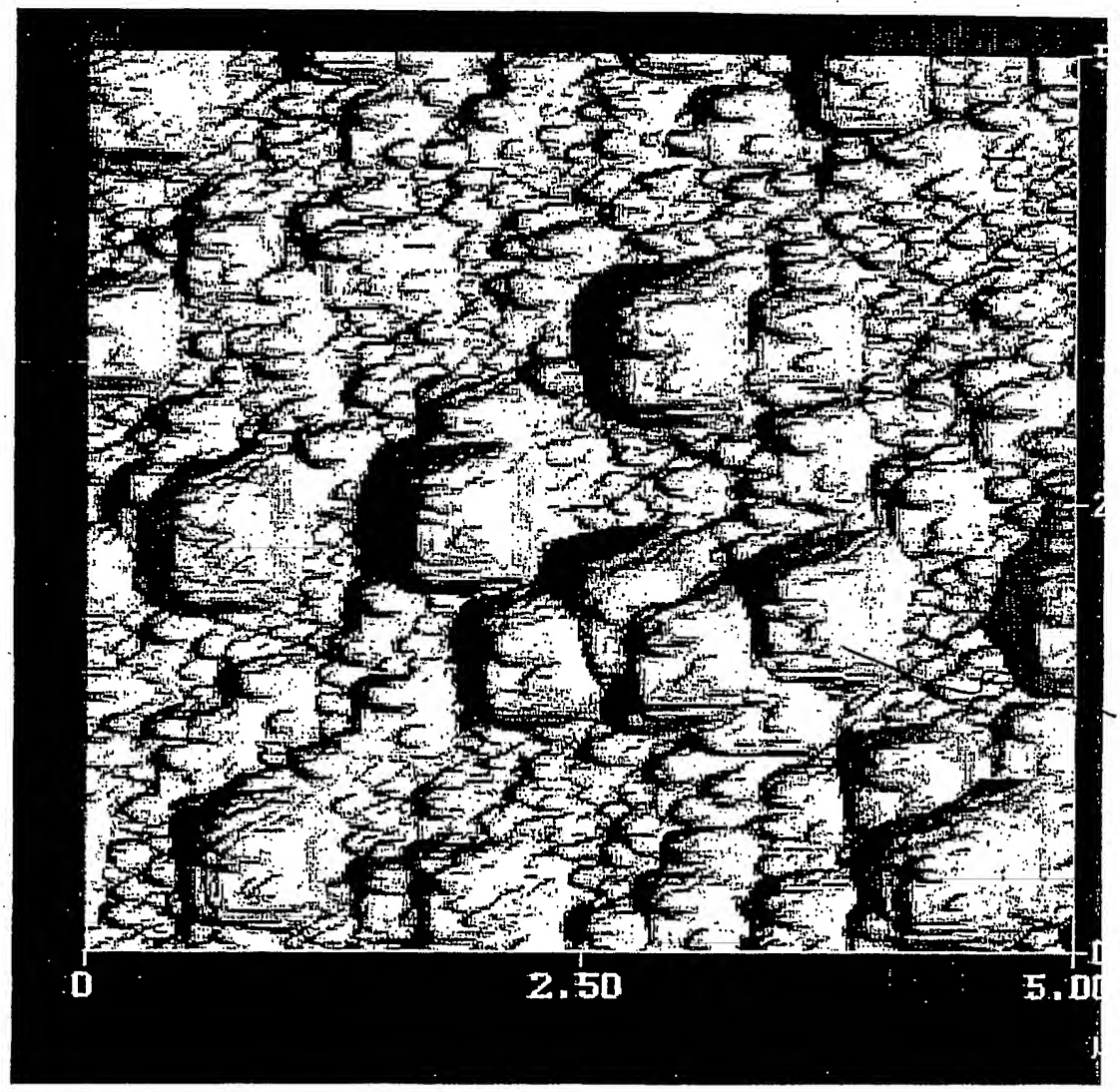

FIGURE 4